**Linear algebraic nodal analysis (LANA) algorithm variable guide**

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Choosing names and notation for mathematical variables is an art. Good notation begets lucid thinking. Bad notation causes unnecessary confusion. This document provides more information and insights about the variables and equations that make up linear algebraic nodal analysis. In some cases, we explore possible noun phrases to refer to relevant equations in written or spoken format. The hope is to improve your capacity to use the LANA algorithm to describe the behavior of electric circuits and set a foundation for you to use linear algebra in engineering contexts.

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## Input: Ideal circuit diagrams labels

The LANA algorithm is designed to provide an authentic modeling experience for anyone interested in learning how to apply linear algebra in engineering contexts. The input to this algorithm is a complete description of an electric circuit that includes resistors along with dc voltage and current sources. At the introductory level, this input usually comes in the form of an ideal circuit schematic. Below are two resources that suggest best practices to draw and label these types of circuit diagrams:

- ☐ Rules and guidelines for drawing good schematics from the Electronics Stack Exchange
- ☐ Guidelines for Drawing Schematics by Tim J. Sobering

When drawing an ideal circuit diagram, we define and label each element using a letter and number combination (eg. R1, V3, I2). We use uppercase English letters to indicate the type of component while the corresponding number enumerates each individual element of this type in the circuit. This convention follows from a similar practice of stamping each ideal element in Computer-Aided Design (CAD) programs. We use the standard letter codes for resistors, voltage sources, and current sources, seen in Table 1 below.

| **Letter Code** | **Element Type** |
|---|---|
| R | Resistor |
| V | Voltage Source |
| I | Current Source |

Table 1: Letters for component labels

To ensure readability and ease of reference, each component designator appears next to the associated component. We dedicate the use of both the lower- and upper-case English letters R, V, and I to represent quantities related to resistance, voltage, and current, respectively. Table 2 below provides examples of the element labels used in the input to the LANA algorithm.

| Element label | Description and notes |
|---|---|
| R3 | *Element label* or *element name* for resistor 3 in an ideal circuit schematic. |
| V1 | *Element label* or *element name* for dc voltage source 1 in an ideal circuit schematic. |
| I2 | *Element label* or *element name* for dc current source 2 in an ideal circuit schematic. |

Table 2: Example element labels for an ideal schematic

 

## Step 1: Identify and label the entire set of nodes of our circuit

There are two main goals for labeling each node. First we want a unique identifier for each node and second we want to count the total number of nodes. In other words, we want to create a bijection between the circuit nodes and a set of natural numbers. In LANA, we do this by labeling the nodes with natural numbers $1, 2, ..., n_g$, where $n_g$ is the total number of nodes in the circuit. This avoids the need to use lowercase letters to refer to the nodes and gets right to the point. Each node label is identical to its corresponding index.

There is one possible downside to this approach. If we're not careful, we can cause confusion when referring to other integers. The sentence

"Edge $e_1$ goes out of node 2 and into node 1."

does a much better job of referring to the nodes in context than the less-clear statement

"Edge $e_1$ goes out of 2 and into 1."

The nonnegative integers play many roles throughout this work so we must be extra careful to refer to each node in the proper context. Assuming we so, labeling the nodes with natural numbers is simple and effective.

### Step 2A: Track the dimensions of key features in our circuit

The digraph model of the electric circuit consists of two sets: the set of nodes $\mathcal{N}$ and the set of edges $\mathcal{E}$. We use math calligraphy typeface to represent all sets that describe directed graphs, as shown in Table 3 below.

| Variable | Description and notes |
|---|---|
| $\mathcal{G}$ | Our *digraph model of the electric circuit* with $\mathcal{G} = (\mathcal{N}, \mathcal{E})$. |
| $\mathcal{N}$ | The *set of nodes* $\mathcal{N} = \{1, 2, ..., n_g\} \subset \mathbb{N}$. We might say these are the *set of nodes that define the digraph* $\mathcal{G}$ or the *set of circuit nodes*. |
| $\mathcal{E}$ | The *set of edges* $\mathcal{E} \subset \mathcal{N} \times \mathcal{N}$. Each edge is an ordered pair of nodes. We call the first coordinate of an edge the *initial node* and the second coordinate the *terminal node*. Each directed edge points out of the initial node into the terminal node. For circuit applications, we say that no *self-loops* are allowed meaning that the initial and terminal nodes cannot be the same. |

Table 3: The sets that describe our directed graph model of the circuit.

Throughout this work, we dedicate the lower case letter $n$ to count the cardinality of special subsets of nodes. Table 4 below highlights variables that rely on the lower case letter $n$.

| **Variable** | **Element Type** |
|---|---|
| $n_g$ | Total number of nodes (including the ground node). |
| $n_f$ | Number of free variables in the voltage-source linear-systems problem. |
| $n$ | Minimal number of independent nodes needed to analyze circuits. |

Table 4: Letters for cardinality for sets of nodes

Notice the special use of subscripts to differentiate between each variable in Table 4. These subscripts are designed as memory tools to call into mind the role of each specific counter, as highlighted in Table 5 below.

| **Subscript** | **Significance** |
|---|---|
| $g$ | Tracks when the ground node is included (g means ground is included). |
| $f$ | Refers to free variables from the voltage-source linear-systems problem. |
| | No subscript Indicates that all constraints have been eliminated. |

Table 5: Letters for cardinality for sets of nodes

We use the lower case letter $m$ counts the cardinality (as a nonnegative integer) of special subsets of edges. Since we establish a bijection between edges of our digraph model and circuit elements, the letter $m$ also counts subsets of circuit components.

The central reason why we choose letters $m$ and $n$ to count edges and nodes comes from conventions in applied linear algebra. Linear algebraists love to write matrix dimensions in the form $m \times n$ where $m, n \in \mathbb{N}$. Lloyd Trefethen and David Bau have a brief description of this convention on page 9 of their famous *Numerical Linear Algebra* textbook in their section titled "A note on $m$ and $n$." With this convention in mind, Table 5 below highlights all of the dimensions used to describe the entire incidence matrix.

| Variable | Description and notes |
|---|---|
| $n_g$ | This positive integer counts the *total number of nodes* in the circuit, including the ground node. In electrical engineering, it is sometimes ambiguous if a node count includes the ground node or not. The subscript $g$ makes it abundantly clear that the ground node is included in this count. When the subscript $g$ is present on the integer $n$, we are counting all $n$odes in the circuit, including the $g$round node |
| $m_r$ | This positive integer represents the *number of resistors* in the circuit. |
| $m_v$ | This nonnegative integer represents the *number of dc voltage sources* in the circuit. |
| $m_i$ | This nonnegative integer represents the *number of dc current sources* in the circuit. |
| $m$ | This positive integer represents the *total number of circuit elements* with $$m = m_r + m_v + m_i.$$ We might also say that this counter represents the *total number of edges* in the digraph model of our circuit or the *cardinality of the edge set* $\mathcal{E}$. |

Table 5: Dimensions for node and edge sets for the entire incidence matrix

**Step 2B: Orient and enumerate the edges of the digraph**

Replace each circuit element with an edge of our digraph. For edges associated with current sources, we orient this edge in the same direction as the flow of current in that source. For edges of our graph corresponding to voltage sources, we orient these edges from the positive "+" lead to the negative "-" lead of the associated sources. Finally, we assign arbitrary directions to all edges corresponding to the resistors in our circuit. In addition to orienting each edge according to the rules outlined above, we also choose a very special enumeration scheme for the edges of our circuit. First we count and label all edges corresponding to resistors as edges $e_1, e_2, ..., e_{m_r}$. Next, we continue our count by labeling the edges corresponding to voltage sources, yielding edges $e_{m_r+1}, ..., e_{m_r+m_v}$. Finally, we enumerate our edges corresponding to current sources as $e_{m_r+m_v+1}, ..., e_m$.

 

## Step 3: Create all circuit matrices

For all circuit equations described below, we follow the well-established convention that boldface, lowercase English letters represent vectors while italicized lowercase letters represent scalar-valued entries within these vectors. Uppercase English letters represent matrices.

### Step 3A: Create the entire incidence matrix

We define the entire incidence matrix with the rows corresponding to edges and the columns corresponding to the nodes. The reason we choose this orientation is to describe nodal analysis using a larger equilibrium equation framework espoused by Gilbert Strang in Chapter 2 of his *Introduction to Applied Mathematics* textbook. This framework suggests the structure $A^TCA$ as the output to our nodal analysis algorithm. If we chose to map rows to nodes and columns to edges, we end up with a matrix structure in the form $ACA^T$. Of course, this alternative approach is completely valid but LANA focuses on illustrating the power in the structure $A^TCA$. Thus we associate edges with rows and nodes with columns. Below are all incidence matrices used to describe the directed graph model from step 2.

| Variable name | Description and notes |
|---|---|
| $A_g$ | This *entire incidence matrix* has $m$ rows and $n_g$ columns. I might also call this the *incidence matrix encoding the circuit's digraph prior to eliminating the ground node.* |
| $A_{r_g}$ | The *resistor subblock of the entire incidence matrix* or the *entire resistor subblock*, with $A_{r_g} \in \mathbb{R}^{m_r \times n_g}$. |
| $A_{v_g}$ | The *entire voltage source subblock* or the *voltage-source subblock of the entire incidence matrix* with $A_{v_g} \in \mathbb{R}^{m_v \times n_g}$. Notice that $m_v$ might be equal to zero if no voltage sources are attached to our circuit. In this case, this subblock is empty. |
| $A_{i_g}$ | The *entire current source subblock* or the *current-source subblock of the entire incidence matrix*, with $A_{i_g} \in \mathbb{R}^{m_i \times n_g}$. Since $m_i$ might be equal to zero if no current sources are attached, this subblock may not exist. |

Table 6: The entire incidence matrix and it's subblocks

### Notes on index variables for the incidence matrices

When referring to specific rows and columns of these incidence matrices, we use index variables. We dedicate the symbol $j \in \mathbb{N}$ to refer rows and letter $k$ to specify nodes. We do not use the letter $i$ as an index. In electrical engineering, the letter $i$ refers to current. There is a valid argument that the letter $j$ may also cause some confusion since many electrical engineers set $j = \sqrt{-1}$. However, since LANA focuses on DC analysis of circuits containing only resistors and dc power sources, we need not dip into complex analysis. Moreover, even if we do decide to use complex numbers, we can specifically reference the use of the letter $j$ as an index variable wherever it appears.

**Step 3B: Create the node voltage potential vector**

Table 7 below presents the variables used to describe the entire set of node voltage potentials in the circuit. In steps 5 and 6 of the LANA algorithm, we impose constrains on some of these variables and reduce this list to a minimal set of potential variables from which all other circuit values can be calculated.

| Variable name | Description and notes |
|---|---|
| $\mathbf{u}_g$ | The *entire list of node voltage potentials* of the circuit with $\mathbf{u}_g \in \mathbb{R}^{n_g}$. This list of voltage potentials assumes we have not yet chosen the ground node. |
| $u_k$ | The *voltage potential of the kth node*, where $u_k = \text{Entry}_k(\mathbf{u}_g)$ for $k \in \{1, 2, ..., n_g\}$. |

Table 7: The node voltage potential variables for the circuit

**Step 3C: Create the voltage drop vector**

| Variable name | Description and notes |
|---|---|
| $\mathbf{v}$ | The *vector of voltage drops across each element* with $\mathbf{v} \in \mathbb{R}^m$. We might also refer to this as the *voltage-drop vector*. |
| $\mathbf{v}_r$ | The *resistor voltage-drop vector* or the *resistor subblock of the vector of voltage drops*, with $\mathbf{v}_r \in \mathbb{R}^{m_r}$. |
| $\mathbf{v}_v$ | The *voltage-source voltage-drop vector* where $\mathbf{v}_v \in \mathbb{R}^{m_v}$. We might also name this vector the *voltage-source subblock of the vector of voltage drops*. Assuming $m_v > 0$, this vector has scalar-valued entries given by $v_{v_j} = \text{Entry}_j(\mathbf{v}_v)$ for $j = 1, ..., m_v$. |
| $v_{v_j}$ | Assuming $m_v \geq 1$, we see $v_{v_j} = \text{Entry}_j(\mathbf{v}_v)$ for $j \in \{1, ..., m_v\}$. The value of $v_{v_j}$ is the assigned value of the circuit element Vj which can be read from the dc voltage sources. We should explicitly note that these values are KNOWN constants. |
| $\mathbf{v}_i$ | The *current-source voltage-drop vector* has the property that $\mathbf{v}_i \in \mathbb{R}^{m_i}$. Another way to refer to this vector might be to use the phrase the *current-source subblock of the vector of voltage drops*. |

Table 8: Voltage-drop variables for each element in the circuit.

**Step 3D: Create the current vector**

| Variable | Variable name, description and notes |
|---|---|
| $\mathbf{i}$ | The *current vector* or the *vector of currents through each element* with $\mathbf{i} \in \mathbb{R}^m$. |
| $\mathbf{i}_r$ | We have $\mathbf{i}_r \in \mathbb{R}^{m_r}$ and we might say this is the *resistor current vector*, the *resistor subblock of the vector of currents through each element*, or the *current vector for the resistors*. |
| $\mathbf{i}_v$ | The *voltage-source current vector*, where $\mathbf{i}_v \in \mathbb{R}^{m_v}$, also referred to as the *voltage-source subblock of the current vector*. |
| $\mathbf{i}_i$ | The *current-source current vector* has the property that $\mathbf{i}_i \in \mathbb{R}^{m_i}$. Another way to refer to this vector might be to use the phrase the *current-source subblock of the vector of currents through each element*. |
| $i_{i_j}$ | Assuming $m_i \geq 1$, we see $i_{i_j} = \text{Entry}_j(\mathbf{i}_i)$ for $j \in \{1, ..., m_i\}$. The value of $i_{i_j}$ is the assigned value of the circuit element Ij which can be read from the dc current sources. We should explicitly note that these values are KNOWN constants. |

Table 9: Current variables for each element in the circuit.

**Step 4A: State the entire set of Kirchhoff's current laws (KCLs)**

| Equation | Equation name, description, and notes |
|---|---|
| $A_g^T \mathbf{i} = \mathbf{0}$ | The *entire set of Kirchhoff's current law equations in matrix form with zero right-hand side*. We might also refer to this equation as the *complete list of KCLs with right-hand side equal to zero*. |
| $A_{r_g}^T \mathbf{i}_r + A_{v_g}^T \mathbf{i}_v = -A_{i_g}^T \cdot \mathbf{i}_i$. | The *subblock form of the entire set of KCLs with nonzero current-source forcing term on right-hand side*. |

Table 10: Matrix equations to express KCL equations.

**Step 4B: State the brach constitutive relations (BCRs)**

Branch constitutive relations (BCRs) are equations that relate the voltage drop across to the current running through a particular circuit element. For the types of circuit's we study in this work, the only type of BCRs are associated with the resistors in the circuit and are known as Ohm's law. We can track two different versions of Ohm's law, as seen in Table 11 below.

| Equation | Equation name, description, and notes |
|---|---|
| $\mathbf{v}_r = R\,\mathbf{i}_r$ | The *resistance form of Ohm's law equations* for all resistors in circuit. Also known as the *matrix version of Ohm's law in resistance form.* |
| $\mathbf{i}_r = G\,\mathbf{v}_r$ | The *conductance form of Ohm's law equations* for all resistors in circuit. Also known as the *matrix version of Ohm's law in conductance form.* |

Table 11: Matrix equations to express Ohm's law.

The individual entries of matrix $R$ come from the assigned values of the resistors, as seen in Table 12 below.

| Variable name | Description and notes |
|---|---|
| $r_j$ | The *assigned resistance value* associated with the $j$th resistor Rj in the circuit for $j = 1, 2, ..., m_r$. This is also known as the *resistance* of the $j$th resistor. |
| $R$ | This $m_r \times m_r$ diagonal matrix, known as the *resistance matrix*, stores the resistances of all resistors as the diagonal elements with $$R = \begin{bmatrix} r_1 & 0 & \cdots & 0 \\ 0 & r_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & r_{m_r} \end{bmatrix}.$$ |
| $G$ | The diagonal matrix $G \in \mathbb{R}^{m_r \times m_r}$ is defined as $G = R^{-1}$. The entry-by-entry definition is given as $$G = \begin{bmatrix} g_1 & 0 & \cdots & 0 \\ 0 & g_2 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & g_{m_r} \end{bmatrix}$$ where $g_j = \frac{1}{r_j}$ for $j \in \{1, 2, ..., m_r\}$. This is also called the *conductance matrix.* |

Table 12: Resistor and conductance variables in Ohm's law equations.

**Note about conductance variables**

A natural thought for mathematicians not trained as electrical engineers is to assume we should name the conductance matrix $C$ instead of $G$. The word conductance starts with the letter "C" and the equilibrium equation framework suggested by Strang also includes matrix $C$. While this is a great thought, it doesn't stand up to the test of making our math as clear as possible for the end users. In electrical engineering, the letter "C" is used for capacitors. Following conventions in electrical engineering, we use the variable $g_j$ to describe the conductance of the $j$th resistor.

**Step 4C: State the entire set of Kirchhoff's voltage laws (KVLs)**

In stating Kirchhoff's voltage laws (KVLs), we choose a convention that is specialized to CAD programming for on circuit simulation. In contrast, most introductory physics and engineering course present KVL equations in two forms. The first form of KVLs is written below.

> The *path form of Kirchhoff's voltage law* states that if two paths in a circuit have the same initial nodes and the same terminal nodes, then the sums of the voltage drops along the two paths must be the same.

The other way to write Kirchhoff voltage law focuses on *loops* instead of paths and reads as follows:

> The *loop form of Kirchhoff's voltage law* states that the sum of all voltage drops around any loop in a circuit must be zero. Alternatively, we might also say that the sum of all voltage rises around any loop in a circuit must be zero.

In the LANA algorithm, we use a more general version of Kirchhoff's voltage laws given as follows:

> The *node-potential form of Kirchhoff's voltage law* states that the voltage drop across any two-terminal element of a circuit is the difference in the node voltage potentials at each lead.

By combining this node-potential KVLs with *circuit matrices* from graph theory, we can produce the other two forms of KVLs as a consequent of this node-potential form. Table 13 below shows how we write the KVLs in node-potential form using the matrices we generated in step 3 of the LANA algorithm.

| Equation | Equation name, description, and notes |
|---|---|
| $A_g \, \mathbf{u}_g = \mathbf{v}$ | The *entire set of Kirchhoff's voltage law equations in node-potential form.* We might also refer to this equation as the *the complete list of KVLs in node-potential form.* |
| $A_{r_g} \, \mathbf{u}_g = \mathbf{v}_r$ | The *entire set of resistor KVLs.* We might also call the equation as the *resistor subblock of the entire set of KVLs.* We stay away from using the terse and less-accurate phrase *resistor KVLs* since the LANA algorithm distinguishes between complete, grounded, and deflated KVL equations, as discussed below. |
| $A_{v_g} \, \mathbf{u}_g = \mathbf{v}_v$ | The *entire set of voltage-source KVL equations* or the *voltage-source subblock of the entire set of KVLs.* The right-hand side of this equation contains known voltage values and this forms the *entire voltage-source general linear-systems problem.* |
| $A_{i_g} \, \mathbf{u}_g = \mathbf{v}_i$ | The *entire set of current-source KVL equations.* We can also refer to this as the *current-source subblock of the entire set of KVLs.* |

Table 13: Matrix equations to express KVLs in node-potential form.

## Step 5: Identify ordinary and generalized nodes

We define a *generalized node* to be any set of nodes connected by a path of voltage sources. For each generalized node, we have only one independent node voltage potential. Any node to which no voltage source is connected is called an *ordinary node*. We use the *deactivated circuit heuristic* to identify ordinary and generalized nodes.

In the deactivated circuit heuristic, we deactivate the voltage and current sources in the circuit by setting their values to zero. This is equivalent to drawing a new *deactivated resistor network* in which we replace each voltage source with a short circuit and each current source with an open circuit. When we deactivate the circuit in this way, the nodes in each generalized node meld together. The node potential variables for all nodes inside a generalized node are constrained by the placement of the voltage sources. Thus, the values of these variables are not independent from each other.

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## Step 6: Create a minimal set of independent node potentials

The LANA algorithm uses linear algebra to reduce the vector $\mathbf{u}_g$ to a minimal set of independent node variables from which all other quantities in the circuit can be calculated. To achieve this reduction, we partition the entries of $\mathbf{u}_g$ into two lists. The first list of *constrained variables* includes one node potential variable for each voltage source and exactly one additional variable for our chosen ground node. The second list of *independent variables* are the chosen node voltage potentials that remain after eliminating the constrained quantities.

### Step 6A: Impose one constraint for each voltage source

To impose the $(m_v + 1)$ constraints, we look at two features of our modeling problem. The first set of constraints is encoded in the element-specific KVLs from step 4C. Specifically, the voltage-source KVLs form a linear-systems problem

$$A_{v_g}\,\mathbf{u}_g = \mathbf{v}_v$$

since the vector $\mathbf{v}_v$ on the right-hand side has known entries. This *voltage source general linear-systems problem* encodes $m_v$ restrictions amongst the entries of $\mathbf{u}_g$. The second type of constraint relates to our choice of ground node. To ground our circuit, we pick a reference node and set one entry of the vector $\mathbf{u}_g$ to zero. By partitioning the entries of $\mathbf{u}_g$ in this way, we create a minimal list $\mathbf{u} \in \mathbb{R}^n$ of independent node variables, where $n = (n_g - m_v - 1)$. To reduce $\mathbf{u}_g$ down to $\mathbf{u}$, we begin with the voltage-source constraints and then we ground the circuit.

| Equation | Equation name, description, and notes |
|---|---|
| $A_{v_g}\,\mathbf{u}_g = \mathbf{v}_v$ | In this *voltage-source subblock of the entire set of KVLs*, we notice that the right-hand side of this equation contains known voltage values. We recognize this as the *voltage-source general linear-systems problem*. We can produce a complete solution to this problem to impose $m_v$ constraints amongst the entries of $\mathbf{u}_g$. |
| $\mathbf{u}_g = \mathbf{p}_g + Z_{v_g}\,\mathbf{u}_f$ | The *complete solution to the voltage-source KVLs.* |

Table 14: Matrix equations to express the voltage-source constraints.

Each variable in the complete solution to the voltage-source general linear-systems problem has special meaning, as show in Table 15 below.

| Variable | Variable name, description and notes |
|---|---|
| $\mathbf{p}_g$ | A *particular solution to the voltage-source KVLs* where $A_{v_g}\,\mathbf{p}_g = \mathbf{v}_v$. |
| $Z_{v_g}$ | The *voltage-source deactivation matrix* of size $n_g \times n_f$. The columns of this matrix form a basis for $\text{Nul}(A_{v_g})$. |
| $n_f$ | The *number of free variables from the voltage-source KVLs*, where $n_f = n_g - m_v$. |
| $\mathbf{u}_f$ | The vector of *free variables* from the voltage-source KVL equations. |

Table 15: Variables to express the voltage-source constraints.

**Step 6B: Impose a single constraint for the ground node**

To impose the final constraint, we choose a single ground node from the remaining $(n_g - m_v)$ free variables and shift the corresponding entry of the vector $\mathbf{u}_f$ from unknown to known. This permits a dimension reduction realized using multiplication with a matrix $D_{f_0} \in \mathbb{R}^{n_f \times n}$. The matrix $D_{f_0}$ is formed by taking the $n_f \times n_f$ identity matrix and deleting the column corresponding to the chosen ground node where

$$n = n_f - 1 = (n_g - m_v) - 1$$

represents the minimum number of node voltage potentials needed to completely analyze the circuit. We use the deflation matrix $D_{f_0}$ to define

$$\mathbf{u} = D_{f_0}^T\,\mathbf{u}_f \qquad \text{and} \qquad Z = Z_{v_g}\,D_{f_0}.$$

**Step 6C: Combine the constraints together**

We then form the *completely reduced solution* to the voltage-source KVLs given by

$$\mathbf{u}_g = \mathbf{p}_g + Z\mathbf{u}$$

where the columns of $Z \in \mathbb{R}^{n_g \times n}$ are in $\text{Nul}(A_{v_g})$ and the vector $\mathbf{u} \in \mathbb{R}^n$ stores the minimal list of independent variables needed to fully analyze the circuit. We sum this up in Table 16 below.

| Equation | Equation name, description, and notes |
|---|---|
| $\mathbf{u}_g = \mathbf{p}_g + Z\,\mathbf{u}$ | *Completely reduced solution* to voltage-source KVLs. |
| $\mathbf{u} = D_{f_0}^T\,\mathbf{u}_f$ | The vector storing a minimal set of independent node voltage potentials needed to analyze the entire circuit. |
| $Z = Z_{v_g}\,D_{f_0}$ | *Grounded voltage-source deactivation matrix* imposes the $(m_v + 1)$ constraints and produce equations in terms of our minimal list of independent node potential variables. |

Table 16: Variables to express the voltage-source constraints.

**Step 7: State and solve the equilibrium equation for the circuit**

| Variable name | Description and notes |
|---|---|
| $A$ | *complete reduced incidence matrix* of size $m \times n$. This describes a digraph model of the deactivated resistor network. We form this *grounded and deactivated incidence matrix* by multiplying $A_g$ on the right by the voltage-source deflation matrix $Z$ with $A = A_g Z$. |
| $A_r$ | This $m_r \times n$ matrix corresponds to the *resistor subblock of the completely reducedincidence matrix* with $A_r = A_{r_g} Z$. We might also refer to this as the *incidence matrix model of the deactivated resistor network.* |
| $A_v$ | This $m_v \times n$ matrix corresponds to the *voltage-source subblock of the maximally deflated incidence matrix* with $A_v = A_{v_g} Z$. By construction, the columns of $Z$ are in the null space of $A_{v_g}$ and we immediately conclude that $$A_v = 0 \in \mathbb{R}^{m_v \times n}.$$ In transpose form, we have $$A_v^T = Z^T A_{v_g}^T = 0 \in \mathbb{R}^{n \times m_v}.$$ In other words, this matrix has all zero entries. We are naming this matrix because it's worth noting that the zero entries result from our construction of the matrix $Z$. |
| $A_i$ | This $m_i \times n$ matrix corresponds to the *current-source subblock of the maximally deflated incidence matrix* with $A_i = A_{i_g} Z$. |

Table 17: Deactivated incidence matrices

| Equation | Equation name, description, and notes |
|---|---|
| $K = A_r^T \cdot G \cdot A_r$ | The *LANA coefficient matrix* also referred to as a *stiffness matrix* associated with our original circuit. |
| $K \cdot \mathbf{u} = A_r^T \cdot G \cdot \mathbf{b} - \mathbf{f}$ | The *linear-algebraic nodal analysis equation.* This is in the exact form espoused by Strang on in box 2E on page 112 of his *Introduction to Applied Mathematics* textbook. The coefficient matrix $K$ is nonsingular and positive definite. |
| $\mathbf{f} = A_i^T \cdot \mathbf{i}_i.$ | The *current source forcing terms on the nodes of the circuit.* In this case, we use same notation outlined in Strang's *Introduction to Applied Mathematics* on page 112. |
| $\mathbf{b} = -A_{r_g}\, \mathbf{p}_g$ | The *voltage-source forcing terms at the nodes of the circuit.* The negative sign matches the notation as outlined in Strang's *Introduction to Applied Mathematics* on page 112. |

Table 18: The Linear Algebraic Nodal Analysis Equation