Step-by-step guide to the linear-algebraic nodal analysis (LANA) algorithm

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INPUT:

Suppose we are given a complete description of an electric circuit containing only resistors, dc voltage sources, and dc current sources. The LANA algorithm proceeds with the steps provided below.

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1. Identify and label the entire set of nodes in our circuit.

   We begin our work by identifying the nodes in our circuit. To do so, we use the *node identification heuristic* in which we erase the element bodies of each ideal circuit element. The contiguous segments of conductor that remain are known as the *nodes* of the circuit. We label the nodes of our circuit using positive integers.

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2. Model the circuit as a directed graph.

   2A. Track the dimensions of key features in our circuit.

   Construct a digraph model $\mathcal{G}$ for our circuit by specifically the dimensions of key features. To do so, we define the following nonnegative integers:

$$\begin{aligned} n_g &= \text{the total number of nodes in the set } \mathcal{N} \text{ (including the ground node)}, \\ m_r &= \text{the number of resistors in the circuit}, \\ m_v &= \text{the number of dc voltage sources in the circuit}, \\ m_i &= \text{the number of dc current sources in the circuit}, \\ m &= \text{the total number of elements in our circuit}. \end{aligned}$$

   Each individual circuit element corresponds to a unique edge in our digraph and the set of edges $\mathcal{E}$ contains exactly m elements, with

$$m = m_r + m_v + m_i.$$

   2B. Orient and enumerate the edges of the digraph.

   Replace each circuit element with an edge in our digraph. If an edge models a current source, we orient this edge in the same direction as the flow of current in that source. We orient an edge that corresponds to a voltage source from the positive "+" lead to the negative "-" lead of the associated source. Finally, we assign arbitrary directions to all edges corresponding to the resistors in our circuit.

   We choose a special enumeration scheme for the edges of our digraph. First, we count and label all edges corresponding to resistors as edges $e_1, e_2, ..., e_{m_r}$. Next, we continue our count by labeling the edges corresponding to voltage sources, yielding edges $e_{m_r+1}, ..., e_{m_r+m_v}$. Finally, we enumerate our edges corresponding to current sources as $e_{m_r+m_v+1}, ..., e_m$. Each time we increment our edge index, we follow the same order determine by the enumeration scheme within each element type given in the original description of our circuit. For example, edge e_i encodes the reference current direction assigned to resistor i for $i = 1, 2, ..., m_r$.

   2C. Draw a directed graph model of the circuit.

3. Create all circuit matrices.

3A. Create the entire incidence matrix

Form the entire incidence matrix $A_g \in \mathbb{R}^{m \times n_g}$ using the entry-by-entry definition

$$a_{jk} = \begin{cases} 1 & \text{if edge } e_j \text{ leaves node } k, \\ -1 & \text{if edge } e_j \text{ enters node } k, \\ 0 & \text{otherwise,} \end{cases}$$

for $j = 1, 2, ..., m$ and $k = 1, 2, ..., n_g$. The rows and columns of this matrix correspond to the edges and nodes of our digraph, respectively. We create a block-partition description of our entire incidence matrix A_g using our enumeration scheme for our digraph's edges, with

$$A_g = \begin{bmatrix} A_{r_g} \\ \hdashline A_{v_g} \\ \hdashline A_{i_g} \end{bmatrix}$$

where the subblocks of this matrix are given by

$$A_{r_g} \in \mathbb{R}^{m_r \times n_g}, \qquad A_{v_g} \in \mathbb{R}^{m_v \times n_g}, \qquad \text{and} \qquad A_{v_g} \in \mathbb{R}^{m_i \times n_g}.$$

3B. Create the node voltage potential vector.

We create the *entire list of node voltage potentials* and store these variables in the vector $\mathbf{u}_g \in \mathbb{R}^{n_g}$. This list of node voltage potentials is organized as a column vector. At this point in the modeling process, we have yet to designate a ground node. Thus, the vector $\mathbf{u}_g$ contains all nodes identified in step 1 of this algorithm.

3C. Create the voltage drop vector.

Define the *voltage-drop vector* $\mathbf{v} \in \mathbb{R}^m$ whose individual entries store the voltage drop across each circuit element, with

$$\mathbf{v} = \begin{bmatrix} \mathbf{v}_r \\ \hdashline \mathbf{v}_v \\ \hdashline \mathbf{v}_i \end{bmatrix} \qquad \text{where} \qquad \mathbf{v}_r \in \mathbb{R}^{m_r}, \ \mathbf{v}_v \in \mathbb{R}^{m_v}, \ \text{and } \mathbf{v}_i \in \mathbb{R}^{m_i}.$$

3D. Create the current vector.

Define the *current vector* $\mathbf{i} \in \mathbb{R}^m$ whose individual entries store the current running through each circuit element, with

$$\mathbf{i} = \begin{bmatrix} \mathbf{i}_r \\ \hdashline \mathbf{i}_v \\ \hdashline \mathbf{i}_i \end{bmatrix} \qquad \text{where} \qquad \mathbf{i}_r \in \mathbb{R}^{m_r}, \ \mathbf{i}_v, \in \mathbb{R}^{m_v}, \ \text{and } \mathbf{i}_i \in \mathbb{R}^{m_i}.$$

4. State the entire set of circuit equations.

4A. State the *entire set of Kirchhoff's current laws* (KCLs).

Finally we state the entire set of KCLs using the equation

$$A_g^T \mathbf{i} = \mathbf{0} \qquad \Leftrightarrow \qquad \left[\begin{array}{c|c|c} A_{r_g}^T & A_{v_g}^T & A_{i_g}^T \end{array} \right] \left[\begin{array}{c} \mathbf{i}_r \\ \hdashline \mathbf{i}_v \\ \hdashline \mathbf{i}_i \end{array} \right] = \mathbf{0}.$$

Since both A_g and $\mathbf{i}$ are block partitioned matrices, we restate our *complete list of KCL's in sublock form* as

$$A_{r_g}^T \mathbf{i}_r + A_{v_g}^T \mathbf{i}_v = -A_{i_g}^T \mathbf{i}_i.$$

4B. State the *brach constitutive relations* (BCRs).

To state the branch constitutive relations for the resistors in our circuit, we use a matrix version of Ohm's law given by the equation

$$\mathbf{v}_r = R \cdot \mathbf{i}_r \qquad \Leftrightarrow \qquad \mathbf{i}_r = G \cdot \mathbf{v}_r$$

where $R \in \mathbb{R}^{m_r \times m_r}$ is a diagonal matrix. Here, we store the appropriate resistance value in each diagonal entry, yielding scalar equations $v_k = r_k \cdot i_k$ for $k = 1, 2, ..., m_r$. Since the kth resistor Rk has positive resistance value $r_k > 0$, we can also rewrite our *Ohm's law equations in conductance form*, where the conductance matrix $G = R^{-1}$ is a diagonal and the main diagonal entries are defined by the individual conductances $g_k = 1/r_k$.

4C. State the *entire set of Kirchhoff's voltage laws* (KVLs).

We recall that the complete set of circuit equations begins with Kirchhoff's voltage law (KVL) in node potential form. In the LANA algorithm, we state this set of equations using matrix multiplication:

$$A_g \, \mathbf{u}_g = \mathbf{v} \qquad \Leftrightarrow \qquad \left[\begin{array}{c} A_{r_g} \, \mathbf{u}_g \\ \hdashline A_{v_g} \, \mathbf{u}_g \\ \hdashline A_{i_g} \, \mathbf{u}_g \end{array} \right] = \left[\begin{array}{c} \mathbf{v}_r \\ \hdashline \mathbf{v}_v \\ \hdashline \mathbf{v}_i \end{array} \right].$$

Using the subblock partition of the entire incidence matrix A_g and the voltage drop vector $\mathbf{v}$, we state the resulting element-specific KVLs as follows:

$$A_{r_g} \, \mathbf{u}_g = \mathbf{v}_r, \qquad A_{v_g} \, \mathbf{u}_g = \mathbf{v}_v, \qquad \text{and} \qquad A_{i_g} \, \mathbf{u}_g = \mathbf{v}_i.$$

4D. Combine the circuit equations.

Using steps 4A, 4B, and 4C, we can re-write the KCL equations in terms of the vector $\mathbf{u}_g$ as follows

$$A_{r_g}^T G A_{r_g} \mathbf{u}_g + A_{v_g}^T \mathbf{i}_v + = -A_{i_g}^T \mathbf{i}_i. \tag{1}$$

with unknown vectors $\mathbf{u}_g$ and $\mathbf{i}_v$.

5. Identify the ordinary and generalized nodes.

   Define a *generalized node* to be any set of nodes connected by a path of voltage sources. Any node to which no voltage source is connected is called an *ordinary node*. To identify ordinary and generalized nodes, we use the *deactivated circuit heuristic* in which we deactivate the power sources by setting the value of each independent source to zero. This is equivalent to drawing a *deactivated resistor network* where we replace the voltage sources with short circuits and current sources with open circuits.

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6. Create a minimal set of independent node potentials.

   6A. Impose one constraint for each voltage source.

   Start with the element-specific KVLs from step 4C and focus on the *voltage-source general linear-systems problem* in the form

$$A_{v_g}\mathbf{u}_g = \mathbf{v}_v.$$

   Produce a complete solution to the voltage-source KVLs in the form

$$\mathbf{u}_g = \mathbf{p}_g + Z_{v_g}\mathbf{u}_f$$

   where $\mathbf{p}_g \in \mathbb{R}^{n_g}$ is a particular solution, the columns of $Z_{v_g} \in \mathbb{R}^{n_g \times n_f}$ form a basis for $\text{Nul}(A_{v_g})$, the dimension $n_f = n_g - m_v$ represents the *number of free variables*, and $\mathbf{u_f} \in \mathbb{R}^{n_f}$ is the vector of free variables.

   6B. Impose a single constraint for the ground node.

   Choose a single ground node from the remaining $(n_g - m_v)$ free variables and shift the corresponding entry of the vector $\mathbf{u}_f$ from unknown to known. Realize this dimension reduction using multiplication with deflation matrix $D_{f_0} \in \mathbb{R}^{n_f \times n}$ where the vector

$$\mathbf{u} = D_{f_0}^T\,\mathbf{u}_f$$

   stores the minimal list of independent variables needed to fully analyze the circuit. The matrix D_{f_0} is formed by taking the $n_f \times n_f$ identity matrix and deleting the column corresponding to the chosen ground node as seen below.

   6C. Combine the constraints together.

   Create the *completely reduced solution* to the voltage-source KVLs given by

$$\mathbf{u}_g = \mathbf{p}_g + Z\mathbf{u} \qquad \text{where} \qquad Z = Z_{v_g}\,D_{f_0}. \tag{2}$$

   The matrix D_{f_0} is formed by taking the $n_f \times n_f$ identity matrix and deleting the column corresponding to the chosen ground node as seen below.

7. State and solve the equilibrium equation for the circuit

   Define matrices

   $$A_r = A_{r_g} Z, \qquad A_{v_g} Z = 0, \qquad \text{and} \qquad A_i = A_{i_g} Z.$$

   Looking back at the combined circuit equations (1) from step 4D, we replace vector $\mathbf{u}_g$ with our completely reduced solution (2) from step 6C. Then we multiply the entire equation (1) on the left-hand side by the matrix Z^T. This yields the matrix equation

   $$A_r^T G A_r \mathbf{u} = A_r^T G \mathbf{b} - \mathbf{f}, \tag{3}$$

   where $\mathbf{b} = -A_{r_g} \mathbf{p}_g$ and $\mathbf{f} = A_i^T \mathbf{i}_i$. Solve this equation using any method. For almost any circuit that is used in real-world applications, the stiffness matrix $K = A_r^T G A_r$ is nonsingular.

OUTPUT:

This algorithm outputs the modeled values for all independent node voltage potentials. We can then use these node potential to solve for any circuit variable we desire.